Three-dimensional TCAD Simulation of n-Type Nanowires Operating at Cryogenic Temperatures down to 20K

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***Abstract*—This paper presents a three-dimensional TCAD simulation study of nanowire MOSFETs operating at cryogenic temperatures. The results are analyzed according to the physical phenomena considered through simulation models, such as carrier ionization. Different MOSFET parameters were monitored to validate the simulations. The results for both carrier ionization models present minimal differences for the threshold voltage and subthreshold slope variations with temperature. Distinctly, the maximum transconductance is reduced in the whole temperature range when incomplete ionization model is used.**

Keywords—nanowires; MOSFET; three-dimensional simulation; cryogenic temperature

I. INTRODUCTION

Since the creation of diodes in the early 1900s, the PN junction in 1939, and the demonstration of transistors in 1947, electronics have gone through great technological advances. Point-contact transistors were first introduced, and later metal oxide semiconductor field effect transistors (MOSFET) were developed. The scientific community then started to study the miniaturization of the MOSFET, and the effects caused on its structure and electrical characteristics. Currently, there are circuits with billions of transistors in each integrated circuit (chip), since even smaller dimensions were reached, on the nanometric scale.

Miniaturization, however, brings problems to the correct functioning of the circuits. Among them are the short channel effects, which deal with the reduction of electrostatic control by the gate electrode between the conduction regions and the channel. Short-channel effects degrade the electrical characteristics of transistors, reducing the threshold voltage and increasing its dependence on the potential applied to the drain, increasing the subthreshold slope and the off-state current [1].

Regarding recent developments, there is an emerging area called quantum computing. With good prospects for becoming the basis of computational simulations, especially when it comes to natural phenomena, it has also shown advantages for data processing such as reduced execution time. Quantum computers, however, rely on classical circuits to extract the processed data and integrate them with the existing electronic systems and the network. Additionally, their basic unit of information is the Qubits, which remain operational only at deep cryogenic temperatures. The Qubits also need control and error correction circuits, which are implemented in CMOS technology [2].

Therefore, it becomes necessary to join two computational technologies in a single system. On the one hand, quantum computing at extremely low temperatures, on the other, the existing CMOS technologies. It has been demonstrated that submitting the CMOS circuitry to cryogenic temperatures, between 1 K and 4 K, contributes to thermal noise and error correction reduction. In this sense, studies are needed to evaluate the functioning of these circuits under these adverse conditions previously not applied to classical computing. Peculiarities such as the non-linearity of the subthreshold slope and the effects of incomplete carrier ionization at cryogenic temperatures are examples of differences concerning these applications [3].

Technology Computer-Aided Design (TCAD) tridimensional simulators are important tools for the CMOS Design Technology Co-Optimization (DTCO), successfully being used for years. However, when the temperature is reduced to the cryogenic range, several problems associated with numerical convergence appear and must be solved [4].

This work aims to carry out TCAD three-dimensional numerical simulations of nanowire MOSFETs operating at different temperatures (T), reaching the cryogenic regime (down to 20 K), to evaluate the coherence of the results. For this, different electrical parameters are analyzed, such as drain-source current (I_{DS}), threshold voltage (V_{TH}), transconductance (gm), maximum transconductance (gm,max), and subthreshold slope (SS).

II. PHYSICAL CHARACTERISTICS AND SIMULATION PARAMETERS

The studied device is a Silicon-On-Insulator (SOI) Ω-gate nanowire n-type MOSFET with similar dimensions to those fabricated in [5]. Table I presents its main geometrical dimensions. Fig. 1 presents the perspective view of the structure, extracted from Sentaurus Visual.

TABLE I. NANOWIRE PHYSICAL DIMENSIONS

Parameter	Dimension [nm]
Fin width (W_{FIN})	10
Fin height (H_{FIN})	10
Channel length (L)	100
Gate-electrode overlap length (L_{OV})	5
Extension length (L_{ext})	10
Equivalent gate oxide thickness	1.3
Buried oxide thickness	145

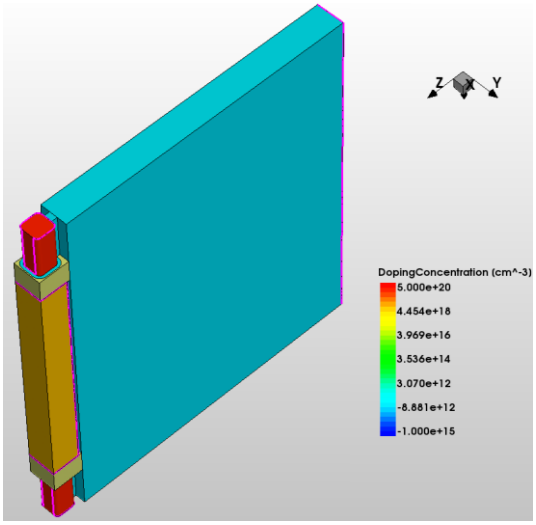

Fig. 1. Perspective view of the studied structure.

The body region is lightly doped p-type with a dopant concentration of $N_A=10^{15}$ cm^{-3}. Also, the simulation structure has n-type source/drain extensions with doping concentration $N_{D,ext}$ = 5 x 10^{19} cm^{-3}. The heavily doped source and drain regions have a doping concentration of N_D = 5 x 10^{20} cm^{-3}.

The three-dimensional numerical simulations were carried out using the Sentaurus Device, from Synopsys, with the default parameters of the simulator [6]. The simulation parameter changed and monitored is the ionization model. The possible ionization models consider either complete or incomplete carrier ionization. All simulations used the Philips and Lombardi mobility models. In addition, it is also utilized extended precision of 128 bits and Box Method.

III. Results

Fig. 2 presents the I_{DS} as a function of V_{GS}, with a drain bias (V_{DS}) of 40 mV, in both linear and logarithm scales, from 35 K to 300 K. These curves were obtained assuming complete carrier ionization in the whole temperature range.

Despite the presence of simulation inaccuracy due to the assumption of complete carrier ionization over temperature, it is possible to observe the Zero Temperature Coefficient (ZTC) point approximately at V_{GS} of 0.56V and I_{DS} of 1.68 µA, where the I_{DS} is independent of the temperature, for temperatures down to 75 K. This point occurs because of the mutual cancellation of the effects of temperature on mobility and threshold voltage [7]. For smaller temperatures, the I_{DS} curves deviate from the ZTC point.

The same simulation has been repeated but turning on the incomplete ionization model. Fig. 3 presents I_{DS} as a function of V_{GS}, with a V_{DS} of 40 mV, in both linear and logarithm scales, from 20 K to 300 K.

The results of Fig. 3 show that the ZTC point is still present for higher temperatures down to 100 K, approximately at V_{GS} of 0.56V and I_{DS} of 1.61 µA. However, the curves obtained at lower temperatures also deviate from the ZTC point, with I_{DS} at 20 K, 25 K, and 35 K smaller than that at 300 K. This indicates the used model parameters for the carrier mobility need to be better adjusted to simulate under extremely low temperatures.

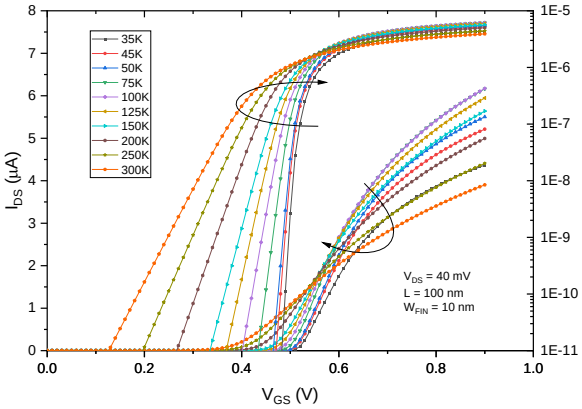

Fig. 2. Curves of the I_{DS} as a function of V_{GS} from 300 K to 35 K, simulated with V_{DS} = 40 mV, for the nanowire with L = 100 nm, W_{FIN} = 10 nm, and complete ionization.

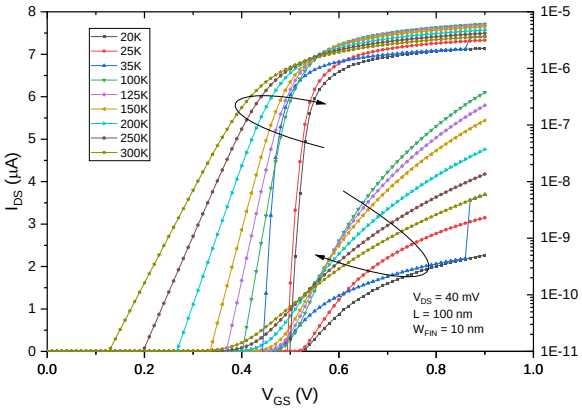

Fig. 3. Curves of I_{DS} as a function of V_{GS} from 300 K to 20 K, simulated with V_{DS} = 40 mV, for the nanowire with L = 100 nm, W_{FIN} = 10 nm, and incomplete carrier ionization.

Fig. 4 shows SS as a function of T for the two previous simulations, considering both complete and incomplete carrier ionization. The values were calculated in the minimum of the

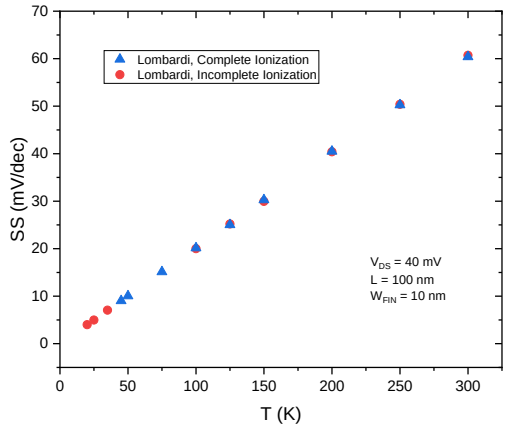

Fig. 4. Curves of the SS as a function of T, simulated with V_{DS} = 40 mV, for the nanowire with L = 100 nm, W_{FIN} = 10 nm, and variable carrier ionization, down to 20 K.

inverse of the logarithm of I_{DS} differentiate with V_{GS} with the transistor operating in subthreshold region [1]. There are missing values due to the simulations not converging.

The results of Fig. 4 show minimal difference between the simulations, therefore a low dependence of SS in terms of the ionization model. They are, for example, accordingly with the theoretical limit for 300 K, approximately 60 mV/dec [8]. However, when approaching lower temperatures, close to cryogenic, the linear behavior is maintained, which is not expected for these conditions. The relation of ln(10).k.T/q is expected to become inaccurate with the increase of the effective density of traps [9].

Fig. 5 presents V_{TH} as a function of T for the same two simulations. The values were calculated using the second derivative method [10].

The results of Fig. 5 are consistent with Fermi potential and the influence of the intrinsic concentration of carriers, showing an inverse linear correlation between V_{TH} and T [11]. The slope values for the linear regression of the data in Fig. 5 are presented in Table II. However, there is minimal difference between the values for the different simulations. This shows that V_{TH} is weakly influenced by the ionization model.

Fig. 6 presents the gm as a function of V_{GS}, from 35 K to 300 K. These curves were obtained assuming complete carrier ionization in the whole temperature range and calculated as the derivative of the I_{DS} versus V_{GS} curve for each temperature.

From Fig. 6, it can be observed the sequential increase of gm with the decrease of the temperature down to 75 K, which can be explained by the reduced carrier scattering [12] increasing the carrier mobility. Distinctly, there is a sequential decrease of gm with the temperature from 50 K to 35 K caused by the increase of the electric field which degrades mobility due to surface scattering [11].

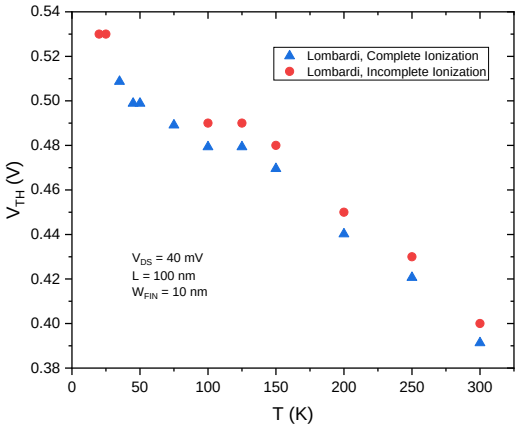

Fig. 5. Curves of V_{TH} as a function of T, simulated with V_{DS} = 40 mV, for the nanowire with L = 100 nm, W_{FIN} = 10 nm, and variable carrier ionization, down to 20 K.

TABLE II. CALCULATED V_{TH} VARIATION RATES ON TEMPERATURE FOR NANOWIRES WITH V_{DS} = 40 MV, L = 100 NM, AND W_{FIN} = 10 NM.

Simulation	dV_{TH}/dT [mV/K]
Lombardi, complete ionization	-0.41
Lombardi, incomplete ionization	-0.46

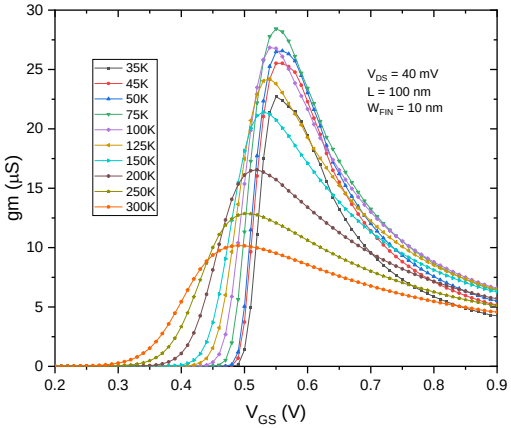

Fig. 6. Curves of gm as a function of T, simulated with V_{DS} = 40 mV, for nanowire with L = 100 nm, W_{FIN} = 10 nm, and complete ionization.

Similarly to the procedure of Fig. 6, Fig. 7 presents the gm as a function of V_{GS}, from 20 K to 300 K, and considering incomplete carrier ionization in the whole temperature range.

Fig. 7 shows the sequential increase of gm with the decrease of the temperature down to 100 K. When comparing the curves of Figs. 6 and 7, it is observed close results for those with the initial inverse relation down to 100 K, while there is a significant difference between the maximum of gm for the temperature of 35 K, which is the lowest common temperature. These results are as expected, considering that incomplete carrier ionization is known to impact MOSFET's parameters, becoming more significant below temperatures of 100 K at which thermal energy is insufficient to cause complete ionization of carriers [8]. For smaller temperatures, there is a degradation in the transconductance. Therefore, the indication remains that the incomplete ionization model with default parameters is not adequate for cryogenic temperatures.

Fig. 8 presents the extracted maximum transconductance (gm,max) as a function of T for the two previous simulations, considering both complete and incomplete carrier ionization.

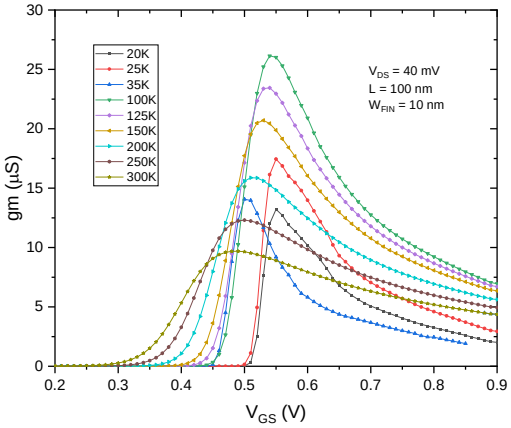

Fig. 7. Curves of gm as a function of T, simulated with V_{DS} = 40 mV, for the nanowire with L = 100 nm, W_{FIN} = 10 nm, and incomplete carrier ionization.

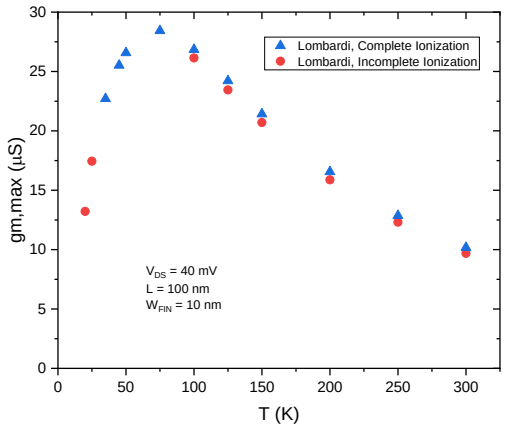

Fig. 8. Curves of the maximum transconductance (gm,max) as a function of T, simulated with V_{DS} = 40 mV, for the nanowire with L = 100 nm, and W_{FIN} = 10 nm.

The values were obtained as the maximum of dI_{DS}/dV_{GS} for each temperature.

From Fig. 8, it can be better observed the minimal difference between the simulations results. However, while considering incomplete ionization, it is possible to say that the peak is near its counterpart, even though it did not converge. Therefore, Fig. 8 shows that the ionization model is unable to yield the differences caused by the incomplete carrier ionization at different temperatures.

IV. Conclusions

This paper presented the TCAD simulation of nanowire MOSFETs at cryogenic temperatures and low drain bias, using default simulator models. The threshold voltage and subthreshold slope variations with temperature are weakly sensitive to the use of incomplete or complete carrier ionization model. For temperatures down to 100 K it is possible to identify the Zero Temperature Coefficient point with both ionization models used. The maximum transconductance reduces with the activation of the incomplete carrier ionization in the whole temperature range. For temperatures lower than 100 K an appreciable degradation in the maximum transconductance is observed, especially if the incomplete carrier ionization model is activated.

Acknowledgment

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